GATE DIELECTRIC ANTIFUSE CIRCUITS AND METHODS FOR OPERATING SAME

ABSTRACT OF THE DISCLOSURE

A number of antifuse support circuits and methods for operating them are disclosed according to embodiments of the present invention. An external pin is coupled to a common bus line in an integrated circuit to deliver an elevated voltage to program antifuses in a programming mode. An antifuse having a first terminal coupled to the common bus line is selected to be programmed by a control transistor in a program driver circuit coupled to a second terminal of the antifuse. The program driver circuit has a high-voltage transistor with a diode coupled to its gate to bear a portion of the elevated voltage after the antifuse has been programmed. The program driver circuit also has an impedance transistor between the high-voltage transistor and the control transistor to reduce leakage current and the possibility of a snap-back condition in the control transistor. A read circuit includes a transistor coupled between a read voltage source and the second terminal to read the antifuse in an active mode. The common bus line may be coupled to a reference voltage through a common bus line driver circuit in the active mode to pass current to or from the read circuit. The common bus line driver circuit has a control transistor and a high-voltage transistor with a diode coupled to its gate to bear the elevated voltage on the common bus line during the programming mode. The read circuit may have a latch circuit to latch a state of the antifuse in a sleep mode. A floating well driver logic circuit raises the voltage potential of wells and gate terminals of p-channel transistors in the read circuit during the programming mode to reduce current flow from the common bus line.